REMARKS

Claims 1-21 were pending in this application.

Claims 1-5, 8-12, and 15-19 have been rejected.

Claims 6, 7, 13, 14, 20, and 21 have been objected to.

Claims 1, 8, and 15 have been amended as shown above.

Claims 1-21 remain pending in this case.

Reconsideration and full allowance of Claims 1-21 are respectfully requested.

I. ALLOWABLE CLAIMS

The Applicants thank the Examiner for the indication that Claims 6, 7, 13, 14, 20, and 21 would be allowable if rewritten in independent form to incorporate all elements of their respective base claims and any intervening claims. Because the Applicants believe that the remaining claims in this application are patentable, the Applicants have not rewritten Claims 6, 7, 13, 14, 20, and 21 in independent form.

II. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-5 and 15-19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,926,052 by Dow et al. ("*Dow*") in view of U.S. Patent No. 6,396,888 by Notani et al. ("*Notani*"). The Office Action rejects Claims 8-12 under 35 U.S.C. § 103(a) as being unpatentable over *Dow* and *Notani* in view of U.S. Patent No. 5,319,679 by Bagby ("*Bagby*"). These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to

make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

Dow recites a circuit and method for producing a phase shifted quadrature signal from an in-phase signal. (*Abstract*). In *Dow*, a phase shifting circuit (element 113) receives an input signal (V_{IN}) and generates an output signal (V_{OUT}). (*Col. 2, Lines 50-59*). The input and output signals are supplied to a phase detector circuit (element 114), which processes the signals and generates a detection signal (V_{DETECT}). (*Col. 2, Lines 60-62*). The detection signal is used by a loop filter circuit (element 115) to generate a control signal ($V_{CONTROL}$), and the control signal is used to adjust the phase shift introduced by the phase shifting circuit (element 113). (*Col. 5, Lines 59 – Col. 6, Line 4*). The function of the loop filter circuit (element 115) is to ensure that the input and output signals are in quadrature. (*Col. 5, Lines 59-62*).

Notani recites a clock recovery circuit for use in a transmission system. (*Col. 18, Lines 25-26; Abstract*). In *Notani*, multiple "variable delay lines" (elements 71 through 7N) process clock signals and generate delayed clock signals. (*Col. 18, Lines 38-41*). The delayed clock signals are then fed through OR gates. (*Col. 18, Lines 41-44*).

The Office Action relies on the phase shifting circuit (element 113) in *Dow* as anticipating the "first current controlled delay line" recited in Claims 1, 8, and 15. (*Office Action, Page 2, Last paragraph*). The Office Action also relies on a phase detector circuit (element 114) in *Dow* as anticipating the "multiplier" recited in Claims 1, 8, and 15. (*Office Action, Page 2, Last paragraph*). The Office Action acknowledges that *Dow* fails to disclose a "delay locked

loop comprising a second current controlled delay line." (*Office Action, Page 2, Last paragraph*).

The Office Action asserts that *Notani* discloses these elements and that it would be obvious to modify *Dow* with the teachings of *Notani*. (*Office Action, Page 2, Last paragraph*). In particular, the Office Action asserts that Figure 18 in *Notani* discloses "a circuit having a first current controlled delay line (7N) and a delay locked loop comprising a second current controlled delay line (71)." (*Office Action, Page 2, Last paragraph*). The Office Action then asserts that it would be obvious to use the delay locked loop (including the variable delay line 71) of *Notani* "as an alternative method for controlling the delay line (113)" of *Dow*. (*Office Action, Page 3, First paragraph*).

As described above, *Dow* already discloses a component – the loop filter circuit (element 115) – that is capable of controlling the phase shifting circuit (element 113). In effect, the Office Action is asserting that it would be obvious to replace the loop filter circuit (element 115) of *Dow* with the delay locked loop of *Notani*.

The loop filter circuit (element 115) of *Dow* processes the detection signal (V_{DETECT}), which is produced by the phase detector circuit (element 114). The only function or purpose of the detection signal (V_{DETECT}) is to be processed by the loop filter circuit (element 115). The only function or purpose of the phase detector circuit (element 114) is to produce the detection signal (V_{DETECT}). As a result, if a modification to *Dow* eliminates the need for the loop filter circuit (element 115) or other component to process the detection signal (V_{DETECT}), the phase detector circuit (element 114) would no longer be needed in the modified *Dow*.

The modification to *Dow* proposed in the Office Action eliminates use of the detection signal (V_{DETECT}). The variable delay line (element 71) in the delay locked loop of *Notani* processes a clock signal. If the loop filter circuit (element 115) of *Dow* is replaced with the delay locked loop of *Notani*, the delay locked loop would process clock signals, and no component of *Dow* would use the detection signal (V_{DETECT}). Because the detection signal (V_{DETECT}) is not needed by any component in the modified *Dow*, the phase detector circuit (element 114) would not be used or included in the modified *Dow*. A person of ordinary skill would not include the phase detector circuit (element 114) in the modified *Dow* because its function is no longer needed.

Moreover, the delay locked loop of *Notani* cannot be modified to process the detection signal (V_{DETECT}) in *Dow*. As noted in the Office Action, the delay locked loop of *Notani* must process a clock signal in order to anticipate the "reference clock signal" recited in Claims 1, 8, and 15. (*Office Action, Page 2, Last paragraph*).

Based on this, if a person of ordinary skill combined *Dow* with the teachings of *Notani* as suggested in the Office Action, the resulting combination would not include the phase detector circuit (element 114). Because the Office Action relies on the phase detector circuit (element 114) to anticipate the "multiplier" recited in Claims 1, 8, and 15, the proposed *Dow-Notani* combination would fail to disclose, teach, or suggest the "multiplier" recited in Claims 1, 8, and 15.

For these reasons, the proposed *Dow-Notani* combination fails to disclose, teach, or suggest the Applicants' invention as recited in Claims 1 and 15 (and their dependent claims).

Also, the proposed *Dow-Notani-Bagby* combination fails to disclose, teach, or suggest the Applicants' invention as recited in Claim 8 (and its dependent claims).

Accordingly, the Applicants respectfully request withdrawal of the § 103(a) rejection and full allowance of Claims 1-5, 8-12, and 15-19.

III. CONCLUSION

For the reasons given above, the Applicants respectfully request reconsideration and full allowance of all pending claims and that this application be passed to issue.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Applicants have included a Petition for Extension of Time and the appropriate fee for a one (1) month extension of time. No additional fees are believed to be necessary. However, in the event that any additional fees are required for the prosecution of this application, please charge any necessary fees to Deposit Account No. 50-0208.

Respectfully submitted,

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